Express Mail Label No.: EV292559876US00
Date of Deposit: November 6, 2003
Docket No.: A0312.70461US00

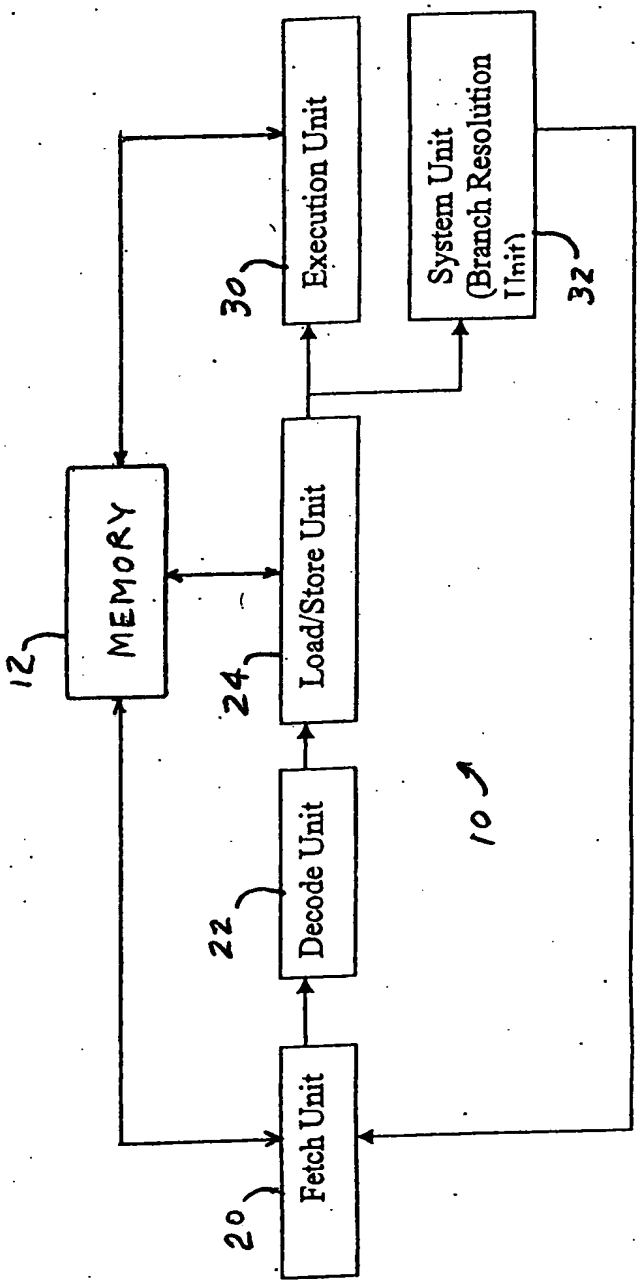

FIG. 1

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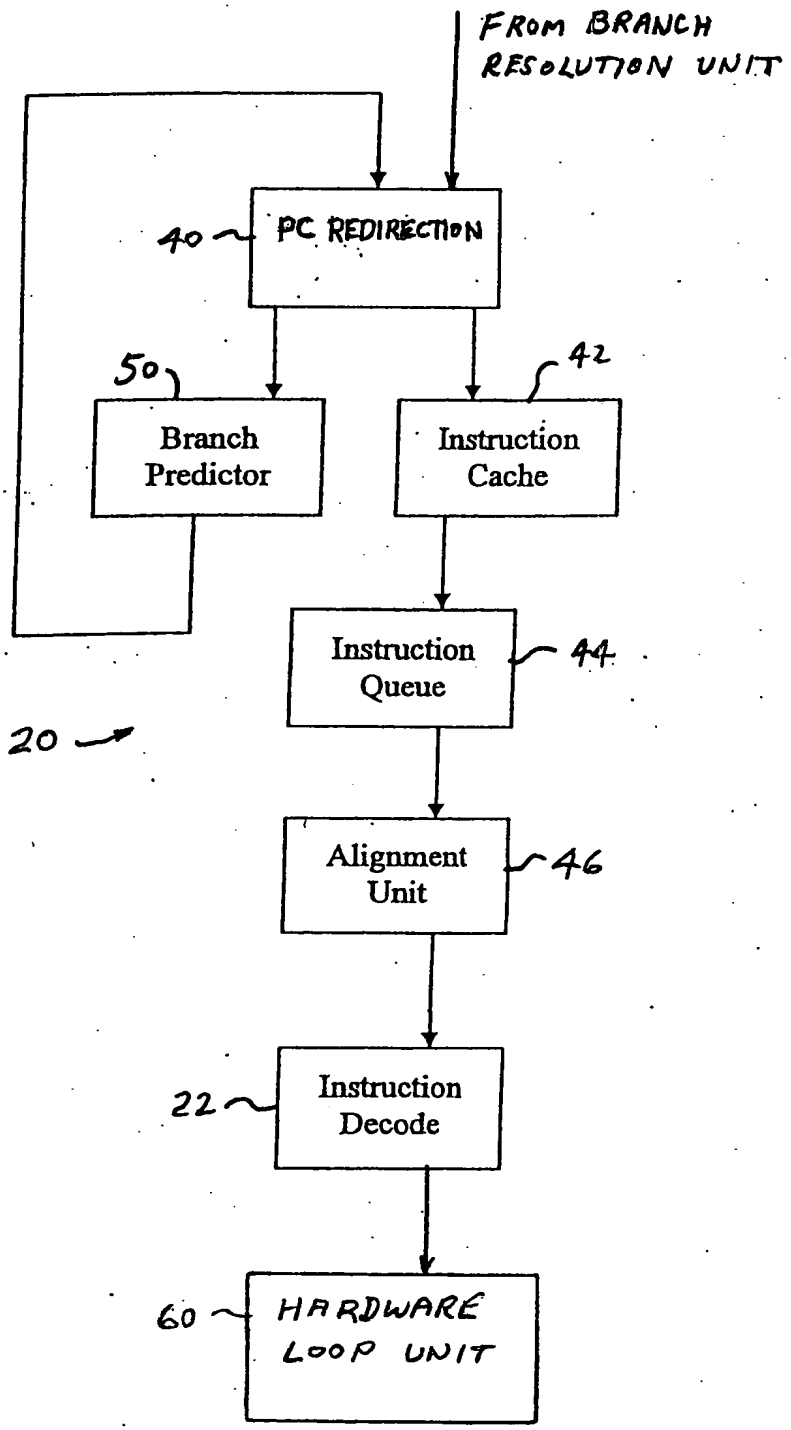

FIG. 2

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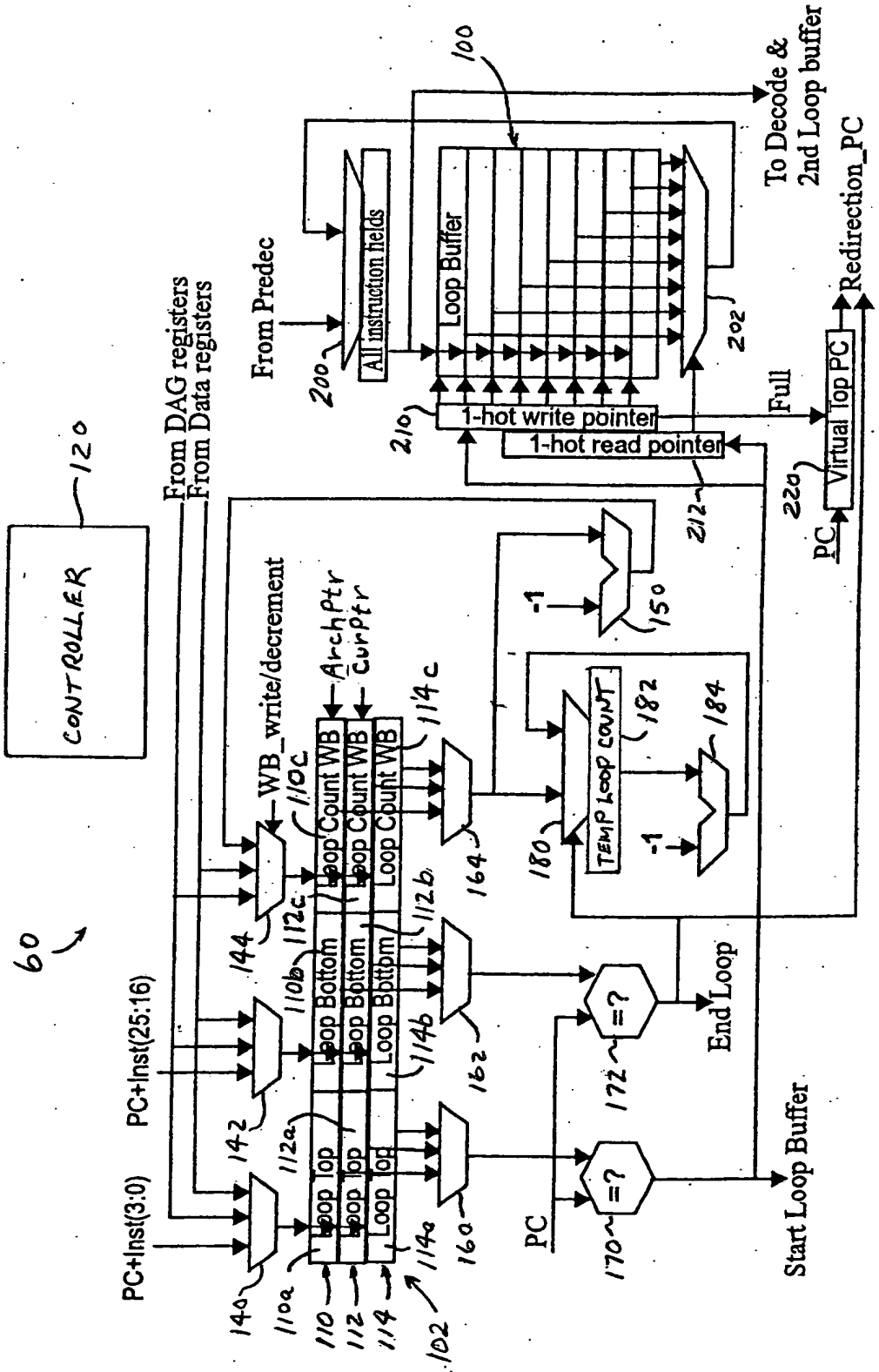

FIG. 3

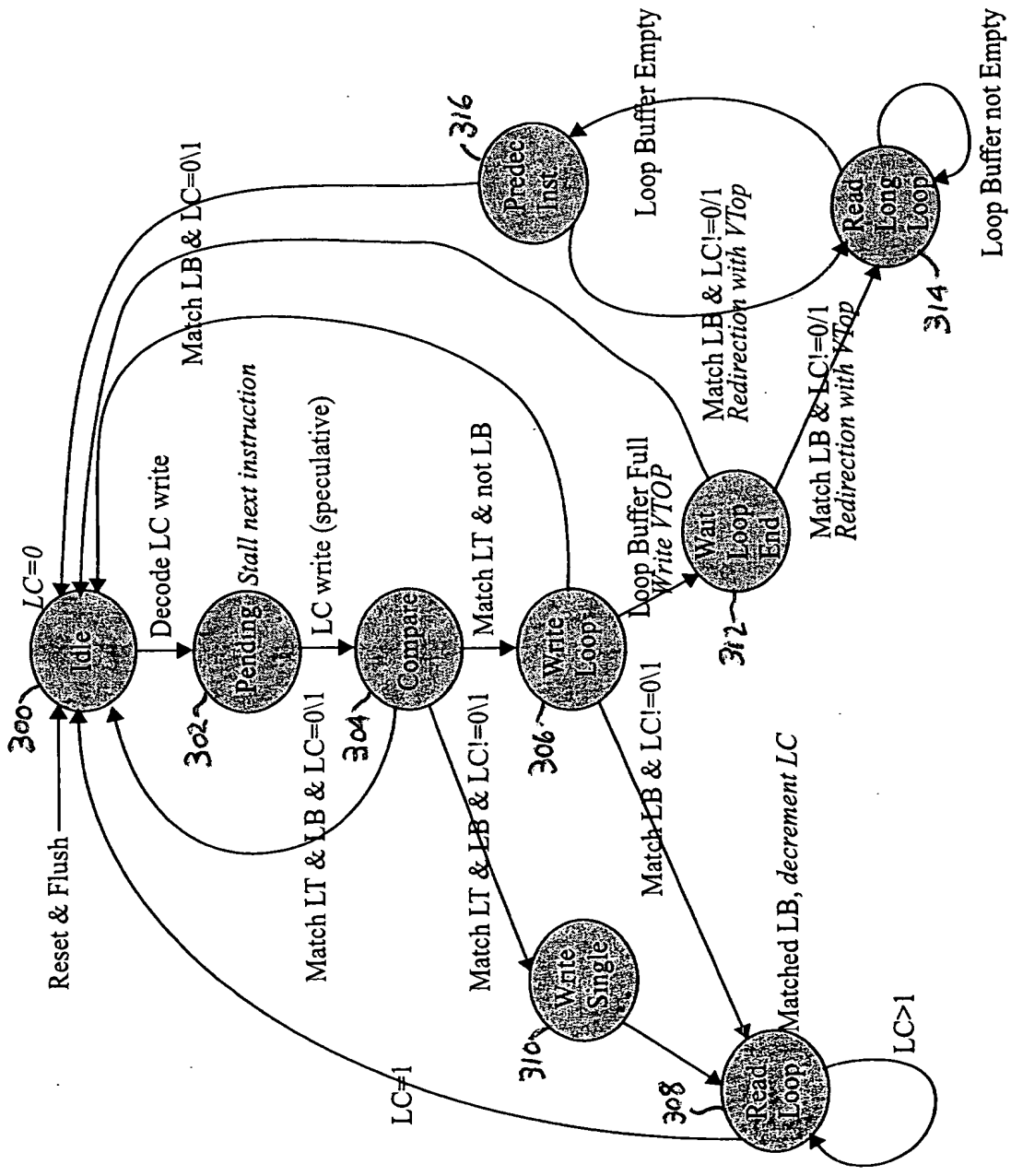
Idle
Pending
Compare
Write Loop
Wait Loop End
Write Single
Read Loop
Predec Inst
Read Long Loop
300
302
304
306
308
310
312
314
316
LC=0
Reset & Flush
Decode LC write
Stall next instruction
LC write (speculative)
Match LT & LB & LC=0\1
Match LT & not LB
Match LT & LB & LC!=0\1
Match LB & LC!=0\1
Loop Buffer Full
Write VTOP
Match LB & LC=0\1
Match LB & LC!=0/1
Redirection with VTop
Loop Buffer Empty
Match LB & LC!=0/1
Redirection with VTop
Loop Buffer not Empty
LC≠1
Matched LB, decrement LC
LC>1

FIG. 4

	Inst	PC(7:0)	Inst Length	Offsets	Next PC	Loop Top	Loop Bottom	Loop Count	Loop Buffer	Comment
400	Lsetup	00110100	32-bit	2/16	00111000	00111000	01010100	Pending	Loopsetup	Loopsetup
401	I1	00111000	16-bit	-	00111010	Match	-	20	write I1	
402	I2	00111010	16-bit	-	00111100	-	-	20	write I2	
403	I3	00111100	16-bit	-	00111110	-	-	20	write I3	
404	I4	00111110	16-bit	-	01000000	-	-	20	write I,4	
405	I5	01000000	16-bit	-	01000010	-	-	20	write I5	
406	I6	01000010	32-bit	-	01000100	-	-	20	write I6	
407	I7	01001000	32-bit	-	01001100	-	-	20	write I7	
408	I8	01001100	64-bit	-	01010100	-	-	20	write I8	
409	I9	01010100	16-bit	-	01010110	-	Match	20	write I9 read I1	set Vtop
410	I1	00111000	16-bit	-	00111010	Match	-	19	read I2	Fetch I9
411	I2	00111010	16-bit	-	00111100	-	-	19	read I3	

FIG,5

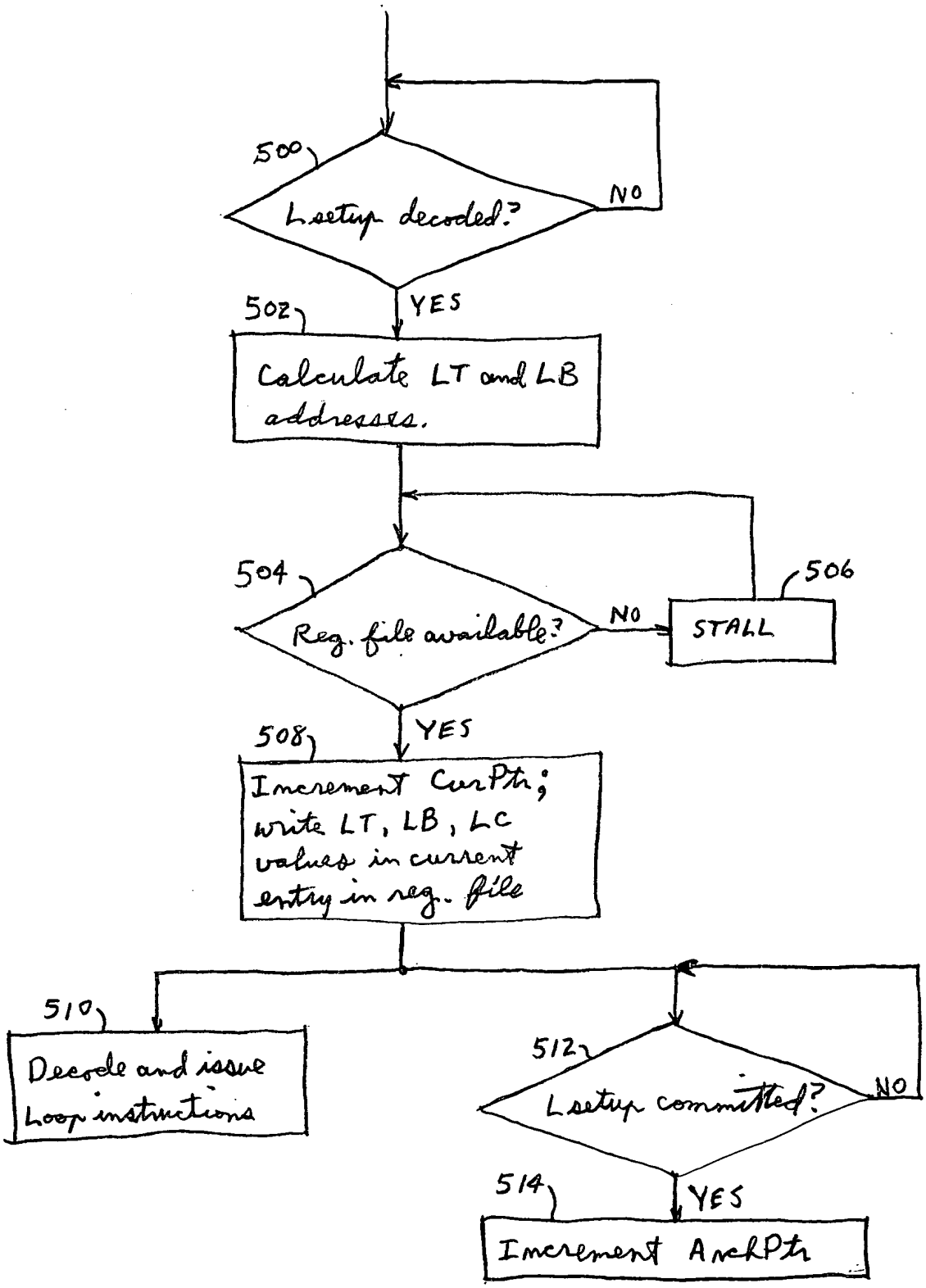
500
L.setup decoded?
NO
YES
502
Calculate LT and LB addresses.
504
Reg. file available?
NO
506
STALL
YES
508
Increment CurPtr; write LT, LB, LC values in current entry in reg. file
510
Decode and issue Loop instructions
512
L.setup committed?
NO
YES
514
Increment AnchPtr

FIG. 6

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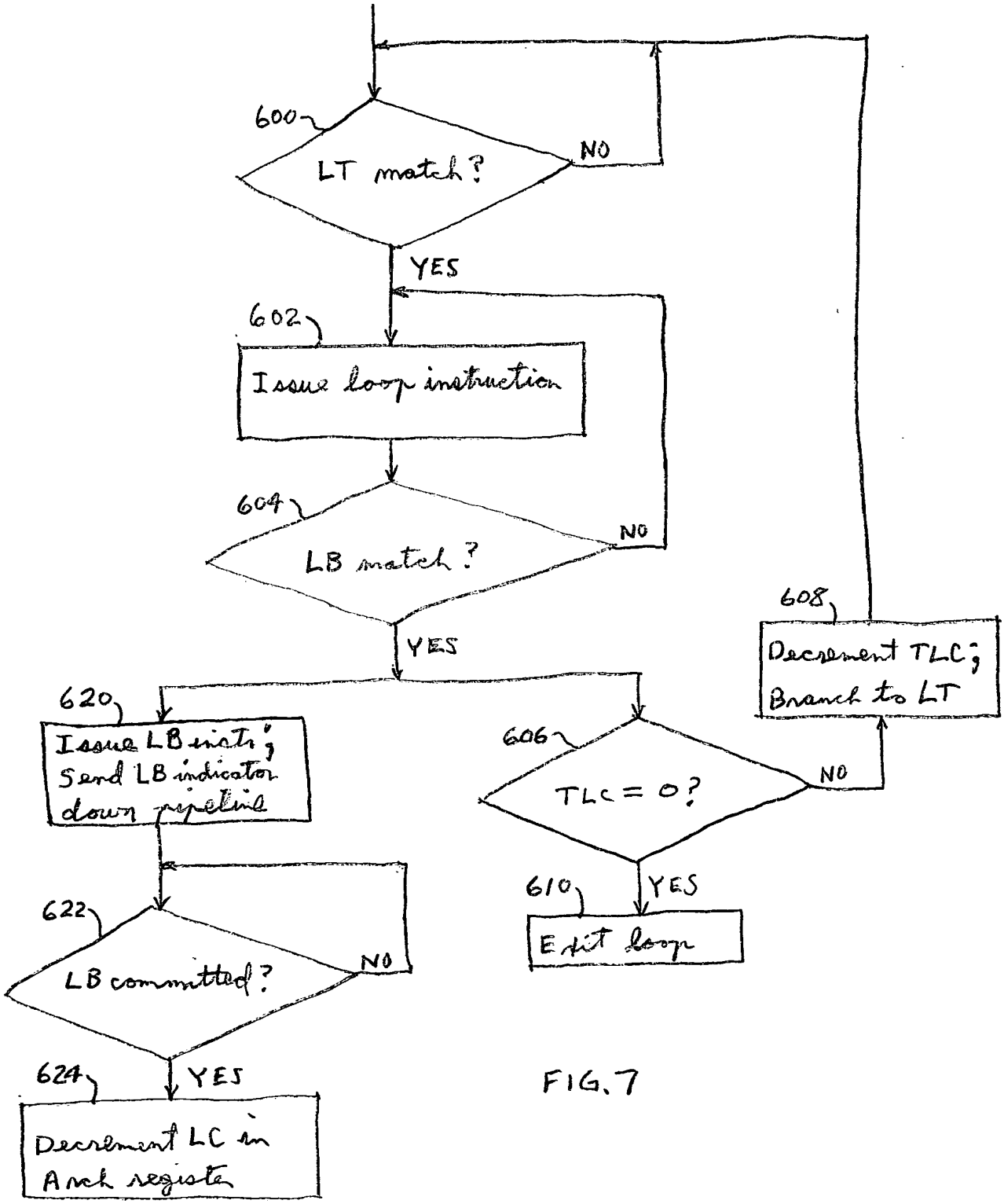

FIG. 7

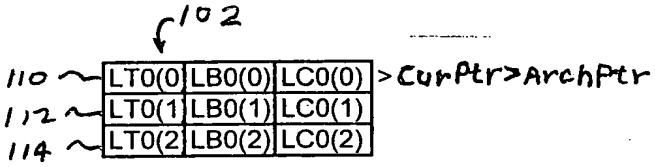

FIG. 8A

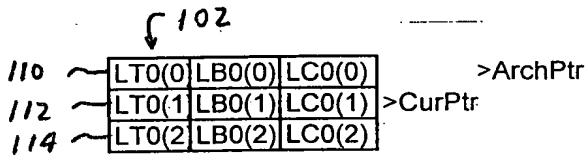

FIG. 8B

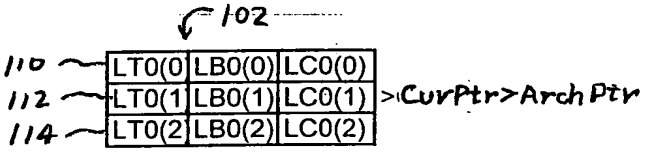

FIG. 8C

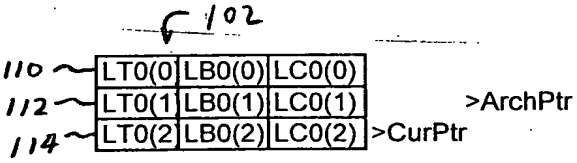

FIG. 8D

Pipe/Cycle	DEC	AC1	AC2	AC3	LS1	LS2	LS3	UC1	LT(0)/LB(0)	TLC/LC(0)	LT(1)/LB(1)	TLC/LC(1)
701 ~ 1	I1	Loop0							PC+2, PC+6	2,2		
702 ~ 2	I2	I1	Loop0						PC+2, PC+6	1,2		
703 ~ 3	I1	I2	I1	Loop0					PC+2, PC+6	1,2		
704 ~ 4	I2	I1	I2	I1	Loop0				PC+2, PC+6	0,2		
705 ~ 5	Loop1	I2	I1	I2	I1	Loop0			PC+2, PC+6	0,2		
706 ~ 6	I4	Loop1	I2	I1	I2	I1	Loop0		PC+2, PC+6	0,2	PC+2,PC+2	0,0
707 ~ 7	I5	I4	Loop1	I2	I1	I2	I1	Loop0	PC+2, PC+6	0,2	PC+2,PC+2	0,0
708 ~ 8	Loop2	I5	I4	Loop1	I2	I1	I2	I1	PC+2, PC+6	0,2	PC+2,PC+2	0,0
Interrupt 709 ~	I6	Loop	I5	I4	Loop1	I2	I1	I2	PC+2, PC+6	0,2	PC+2,PC+2	0,0
710 ~ 10		-	-	-	-	-	-	-	PC+2, PC+6	2,2	-	-

FIG.9